Amendments to the Specification

Please replace the paragraph beginning on page 10, line 7 with the following amended paragraph:

In each of memory blocks MBKL and MBKR, memory cells are arranged in rows and columns. A bit line pair is arranged in correspondence [[too]] to each memory cell column, and a bit line precharge/equalization circuit is arranged in correspondence to each bit line pair. A bit line equalization instruction signal EQL is applied to the bit line precharge/equalization circuit of memory block MBKL, while a bit line equalization instruction signal EQR is applied to the bit line precharge/equalization circuit of memory block MBKR.

Please replace the paragraph beginning on page 13, line 33 with the following amended paragraph:

A case where bit line isolation gate BTGR is maintained in a conductive state in accordance with bit line isolation instruction signal BLIR at high voltage VPP level in the standby state will be considered. In this state, in bit line precharge/equalization circuit BEQR, when precharge voltage VBL is transmitted to bit line BLR through MIS transistor NQ7, a leakage current Ir flows to word line WLR at negative voltage level through high resistance RZ. When the voltage level of bit line BLR lowers, the voltage drop of bit line BLR is transmitted to bit line /BLR through equalization transistor NQ6, whereby the voltage level of bit line /BLR lowers and a current flows from precharge transistor NQ8 to bit line /BLR, accordingly. When word line WLR in the standby state is at negative voltage VBB level particularly, a voltage applied across high resistance RZ is VBL-VBB ~~BVL-VBB~~ and leakage current Ir increases. When bit line precharge/equalization circuit BEQR cannot compensate for leakage current Ir, the voltage drop of bit lines BLR and /BLR

increases. In the worst case, the voltage levels of bit lines BLR and /BLR lowers to negative voltage VBB level.

Please replace the paragraph beginning on page 16, line 8 with the following amended paragraph:

In this standby state, particularly in the standby state in a self refresh mode set in the data holding mode, bit line isolation gate BTGR is set to an off state, making it possible to prevent a current from flowing from sense amplifier SA to high resistance RZ through common bit line CBL. By reducing transistors [[QN6]] NQ6 to NQ8 in size (making the ratio of a channel width to a channel length of each transistor smaller), it is possible to decrease the leakage current in bit line precharge/equalization circuit BEQR.

Please replace the paragraph beginning on page 17, line 17 with the following amended paragraph:

At time T0, an active cycle starts and a memory cell row select operation is carried out. In this case, a memory block including a selected memory cell is first selected in accordance with an address signal. In this example, memory cell MCR shown in Fig. 4 is selected. The level of sense equalization instruction signal EQ is lowered to L level (ground voltage level) in accordance with the deactivation of bit line equalization instruction signal EQR [[BEQR]]. Further, the level of bit line isolation instruction signal BLIL falls from high voltage VPP level to ground voltage GND level, so that bit line isolation gate BTGL is made nonconductive. Accordingly, common bit lines CBL and /CBL are isolated from bit lines BLL and /BLL, respectively. In this state, bit line

precharge/equalization circuit BEQL is active in accordance with bit line equalization instruction signal EQL.

Please replace the paragraphs on page 21, lines 13-32 with the following amended paragraphs:

When bit line isolation instruction signal BLIR is driven to high voltage VPP level, bit lines BLR and /BLR are coupled to common bit lines CBL and /CBL, respectively. The parasitic capacitances of bit lines BLR and /BLR are greater than those of respective common bit lines CBL and /CBL. Therefore, even if the levels of common bit lines CBL and /CBL change from predetermined precharge voltage [[VBLL]] VBL level in the standby state, they are driven to the original precharge voltage level by the precharge voltages of bit lines BLR and /BLR, respectively.

At time T11, word line WLR is driven to be selected and a voltage difference is generated between bit lines BLR and /BLR ~~BLIR and /BLIR~~. The voltage difference between bit lines BLR and /BLR ~~BLIR and /BLIR~~ is transmitted to common bit lines CBL and /CBL.

When the voltage difference between bit lines BLR and /BLR ~~BLIR and /BLIR~~ is sufficiently developed, then sense amplifier activation signals S0N and ZS0P are activated, sense common source nodes S2N and S2P are driven to ground voltage GND level and array power supply voltage VddS level, respectively and sense amplifier SA is activated at time T12. Accordingly, the voltage difference between bit lines BLR and /BLR ~~BLIR and /BLIR~~ is amplified and bit lines BLR and /BLR ~~BLIR and /BLIR~~ are driven to array power supply voltage VddS level and ground voltage GND level, respectively.